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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,104	09/17/2003	Toshinari Takayanagi	004-9196	3693

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,104	TAKAYANAGI, TOSHINARI	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,24-26,45-50 and 56-58* is/are rejected.

7)☒ Claim(s) *2-23,27-44 and 51-55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/8/05, 7/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 10/18/2005 has been entered.

2. Claims 1-58 are presented for examination.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 10/18/2005.

Information Disclosure Statement (IDS) filed on 07/9/2004.

4. Information disclosed and list on PTO 1449 was considered.

Drawings

5. The drawings were received on 09/17/2003. These drawings are acceptable.

Response to Arguments

6. Applicant's arguments with respect to claims1-58 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 24-26,45-50,56-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Winters (U.S. Patent no. 5,515,310).

Regarding claims 1, 24, Winters discloses a circuit (Figure 3) comprising:

first and second matched devices (Figure 3) , which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices (Column 4, lines 40-57) , said shift giving rise to a mismatch in the characteristic between the matched devices (Column 4, lines 17-67); and

a preconditioning circuit (Column 6, lines 25-34) for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device (Column 4, lines 45-57).

Regarding claims 25-26, Winter discloses the first and second matched devices together comprises a cross-coupled pair of transistors (ABSTARCT) within a sensing circuit of a semiconductor memory (Column 5, lines 33-34), and the cross-coupled pair of transistors comprise PMOS transistors (Figure 3, 10,30,20,40).

Regarding claims 45-47, Winters discloses a sensing circuit (Column 5, line 33-34), and including memory (Column 6, line 23), and embodied as a sensing in a computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit (Column 1, lines 20-21).

Regarding claims 48, Winters discloses an integrated circuit comprising:

a memory elements (ABSTRACT);

first and second matched devices (Figure 3) , which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices (Column 4, lines 40-57) , said shift giving rise to a mismatch in the characteristic between the matched devices (Column 4, lines 17-67); and

a preconditioning circuit (Column 6, lines 25-34) for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device (Column 4, lines 45-57).

Regarding claims 49-50, Winters discloses the first and second matched devices together comprises a cross-coupled pair of transistors (ABSTRACT) within a sensing circuit of a semiconductor memory (Column 5, lines 33-34), and the cross-coupled pair of transistors comprise PMOS transistors (Figure 3, 10,30,20,40).

Regarding claims 56-58, Winters disclose a computer readable encoding of a semiconductor integrated circuit design (Figure 3) comprising:

one or more medial encoding a representation of memory circuit that includes plural pairs of bit lines (Figure 3, 14, 16) , memory cells coupled to respective ones of the bit line pairs;

the one or more media further encoding a representation of sense amplifier circuit (Figure 3) coupled to one or more respective ones of the bit line pairs of sensing data stored in associated memory elements, said sense amplifier circuit including first and second matched devices (Figure 3, 10,30,20,40) , which are susceptible to an

accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices (Column 4, lines 40-57) , said shift giving rise to a mismatch in the characteristic between the matched devices (Column 4, lines 17-67); and

the one or more media further encoding a representation of a preconditioning circuit (Column 6, lines 25-34) for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device (Column 4, lines 45-57), and wherein each of the one or more media are selected from the set of a disk, tape or other magnetic, optical, semiconductor or electronic storage medium and a network, wireline, wireless or other communication medium (Column 1, lines 20-21), and in combination with one or more respective media readers therefor, wherein the one or more media and respective media reader, when combined, are exercisable to supply an information stream suitable to at least partially define one or more process steps for fabrication of semiconductor integrated circuits in accordance with the encoded design (Column 1, lines 20-21).

Allowable Subject Matter

9. Claims 2-23,27-44,51-55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-23,27-44,51-55 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or

suggest the claimed limitations. Winters (U.S. Patent No. 5,515,310), and others, does not teach the claimed invention having a preconditioning circuit comprises means for applying a substantially uniform bias history across both first and second matched devices, and a means for subjecting each of the matched devices to substantially equal time durations of predetermined bias condition knows to promote the shift in the characteristic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827